Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2139	netlist	USPAT	OR	OFF	2005/09/01 08:39
S2	764	netlist and digital and power	USPAT	OR	OFF	2005/08/29 07:42
S3	293	netlist and digital and (power adj3 (consumption or usage))	USPAT	OR	OFF	2005/08/29 09:27
S4	148	netlist and digital and (power adj3 (consumption or usage)) and switching	USPAT	OR	OFF	2005/08/29 11:14
S5	11	digital and (power adj3 (consumption or usage)) and (toggle adj3 count)	USPAT	OR	OFF	2005/08/29 11:14
S6	7975	measure$ and digital and (power adj3 (consumption or usage)) and switching	USPAT	OR	OFF	2005/08/29 11:14
S7	3	digital and (power adj3 (consumption or usage)) and (toggle adj3 count) and measure$	USPAT	OR	OFF	2005/08/29 12:39
S8	0	"10802032".an.	USPAT	OR	OFF	2005/08/29 12:39
S9	0	"10802032".pn.	USPAT	OR	OFF	2005/08/29 12:39
S10	0	"10084145".pn.	USPAT	OR	OFF	2005/08/29 12:39
S11	0	"\084145".pn.	USPAT	OR	OFF	2005/08/29 12:39
S12	0	"084145".pn.	USPAT	OR	OFF	2005/08/29 12:40
S13	1	("6876941").PN.	USPAT; USOCR	OR	OFF	2005/08/29 12:40
S14	0	("802032.ap.").PN.	USPAT; USOCR	OR	OFF	2005/08/29 12:40
S15	0	("802032.ap.").PN.	USPAT; USOCR	OR	OFF	2005/08/29 12:40
S16	3	"802032".ap.	USPAT	OR	OFF	2005/08/29 12:41
S17	0	"10802032".ap.	USPAT	OR	OFF	2005/08/29 12:41
S18	3	"802032".ap.	USPAT	OR	OFF	2005/08/29 12:51
S19	0	"802032".apn.	USPAT	OR	OFF	2005/08/29 12:51
S20	0	"10802032".apn.	USPAT	OR	OFF	2005/08/29 12:51
S21	0	"10802032".apn.	USPAT	OR	OFF	2005/08/29 12:52
S22	0	"10802032".APN.	USPAT	OR	OFF	2005/08/29 12:52
S23	0	"10448331".APN.	USPAT	OR	OFF	2005/08/29 12:55
S24	0	"10118427".APN.	USPAT	OR	OFF	2005/08/29 12:55
S25	2	(("6937170") or ("6237132") or ("5563928")).PN.	USPAT; USOCR	OR	OFF	2005/08/29 15:14
S26	3	(("6397170") or ("6237132") or ("5563928")).PN.	USPAT; USOCR	OR	OFF	2005/08/29 15:14

S27	2432	time and (power adj3 (consumption or usage or estimation)) and digital and emulat$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 07:47
S28	40	time and (power adj3 (estimation)) and digital and emulat$5 and hardware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 07:54
S29	1763	power adj3 estimation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 07:55
S30	92	S29 and (digital adj3 circuits)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 07:55
S31	26	S30 and ((toggle adj3 count) or (switching adj3 activity))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 08:17
S32	2	(switching adj3 activity) and (logic adj3 analyzer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:50
S33	3997	netlist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 08:49
S34	1273090	digital	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:28

S35	1763	power adj3 estimation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:29
S36	35	S35 and ((toggle adj3 count) or (switching adj3 activity)) and hardware	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:37
S37	2	("0580495").PN.	USPAT; USOCR	OR	OFF	2005/08/31 09:38
S38	0	("9580495").PN.	USPAT; USOCR	OR	OFF	2005/08/31 09:38
S39	0	"580495.an"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:38
S40	0	"580495.an."	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:38
S41	0	"580495".an.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:38
S42	0	"580495".apn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:39
S43	0	"09580495".apn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:39
S44	4	"580495".ap.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:40

S45	0	"580495".apn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 09:40
S46	3	((toggle adj3 count) or (switching adj3 activity)) and (logic adj3 analyzer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 10:27
S47	43	((toggle adj3 count) or (switching adj3 activity)) and software and (power adj2 estimation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 10:54
S48	43	((toggle adj3 count) or (switching adj3 activity)) and software and (power adj2 estimation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/31 10:54
S49	1	("6151568").PN.	USPAT; USOCR	OR	OFF	2005/09/01 08:39
S50	11	("5426591" | "5481484" | "5487018" | "5493508" | "5515302" | "5517132" | "5519627" | "5526277" | "5541849" | "5555201" | "5557531").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:49
S51	0	"5426591".PN. and (user adj3 input$)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:43
S52	0	"5426591".PN. and (user adj3 input$)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:43
S53	0	("5426591".PN.) and (user adj3 input$)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:43
S54	0	("5426591".PN.) and (user adj3 input$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:46
S55	1	("5555201".pn.) and (user adj3 input)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:47
S56	1	("5557531".pn.) and (user adj3 input)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:47

S57	0	(("5426591" | "5481484" | "5487018" | "5493508" | "5515302" | "5517132" | "5519627" | "5526277" | "5541849" | "5555201" | "5557531").PN.) and ((toggle adj3 (activity or count)) or (switching adj3 activity))	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:50
S58	15932	simulat$ and (time adj3 interval) and input	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:51
S59	3	simulat$ and (time adj3 interval) and (toggle adj3 count)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/01 08:51
S60	3	simulat$ and (time adj3 interval) and (toggle adj3 count)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/01 08:51

Terms used **toggle count power consumption** Found **110** of **160,906**

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1 A hybrid approach for core-based system-level power modeling
Tony Givargis, Frank Vahid, Jörg Henkel
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**
Full text available: pdf(128.11 KB) Additional Information: full citation, references, citings

2 Architectures for cryptography and security applications: Simulation models for side-channel information leaks
Kris Tiri, Ingrid Verbauwhede
June 2005 **Proceedings of the 42nd annual conference on Design automation**
Full text available: pdf(244.28 KB) Additional Information: full citation, abstract, references, index terms

Small, embedded integrated circuits (ICs) such as smart cards are vulnerable to so-called side-channel attacks (SCAs). The attacker can gain information by monitoring the power consumption, execution time, electromagnetic radiation and other information that is leaked by the switching behavior of digital CMOS gates. Ever since power attacks have been introduced in 1999, many countermeasures have been proposed. Often a significant increase in security has been touted. We will show that in order t ...

Keywords: countermeasure, differential power analysis, encryption, security IC, side-channel attack, simulation model, smart card

3 Power estimation approach for SRAM-based FPGAs
Karlheinz Weiß, Carsten Oetker, Igor Katchan, Thorsten Steckstor, Wolfgang Rosenstiel
February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**
Full text available: pdf(846.14 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the power consumption estimation for the novel Virtex architecture. Due to the fact that the XC4000 and the Virtex core architecture are very similar, we used the basic approaches for the XC4000-FPGAs power consumption estimation and extended that method for the new Virtex family. We determined an appropriate technology-dependent power factor Kp to calculate the power consumption on Virtex-chips, and developed a special benchmark test design to condu ...

4 Power estimation of cell-based CMOS circuits
Alessandro Bogiolo, Luca Benini, Bruno Riccò
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Full text available: pdf(218.93 KB) Additional Information: full citation, references, citings, index terms

5 System level issues: Energy characterization of a tiled architecture processor with on-chip networks
Jason Sungtae Kim, Michael Bedford Taylor, Jason Miller, David Wentzlaff
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**
Full text available: pdf(309.58 KB) Additional Information: full citation, abstract, references, citings, index terms

Tiled architectures provide a paradigm for designers to turn silicon resources into processors with burgeoning quantities of programmable functional units and memories. The architecture has a dual responsibility: first, it must expose these resources in a way that is programmable. Second, it needs to manage the power associated with such resources.We present the power management facilities of the 16-tile Raw microprocessor. This design selectively turns on and off 48 SRAM macros, 96 functional u ...

Keywords: power, raw microprocessor, scalar operand network, tile

6 Power-simulation of cell based ASICs: accuracy-and performance trade-offs
D. Rabe, G. Jochens, L. Kruse, W. Nebel
February 1998 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(103.80 KB) Publisher Site Additional Information: full citation, references, citings, index terms

Keywords: Power-Simulation, Power-Estimation, Power-Modelling, Delay-Modelling, Timing-Modelling

7 Poster Session 2: Odd/even bus invert with two-phase transfer for buses with coupling
Yan Zhang, John Lach, Kevin Skadron, Mircea R. Stan
August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**
Full text available: pdf(239.83 KB) Additional Information: full citation, abstract, references, citings, index terms

The coupling capacitances between on-chip bus lines become dominant in deep-submicron technologies. Coding to reduce the *switching activity* of the individual lines was enough to reduce power on buses in older technologies, but new coding techniques that reduce the *coupling activity* between lines are needed for deep-submicron buses. One such coding technique uses the simple observation that coupling capacitances are always charged and discharged by activity on neighboring bus lines, ...

Keywords: bus invert, buses with coupling, coding for low-power I/O

8 Automating RT-level operand isolation to minimize power consumption in datapaths

M. Münch, B. Wurth, R. Mehra, J. Sproch, N. Wehn
January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(116.10 KB) Publisher Site
Additional Information: full citation, references, citings, index terms

9 Survey of code-size reduction methods
Árpád Beszédes, Rudolf Ferenc, Tibor Gyimóthy, André Dolenc, Konsta Karsisto
September 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 3

Full text available: pdf(443.89 KB) Additional Information: full citation, abstract, references, index terms

Program code compression is an emerging research activity that is having an impact in several production areas such as networking and embedded systems. This is because the reduced-sized code can have a positive impact on network traffic and embedded system costs such as memory requirements and power consumption. Although code-size reduction is a relatively new research area, numerous publications already exist on it. The methods published usually have different motivations and a variety of appli ...

Keywords: code compaction, code compression, method assessment, method evaluation

10 Peak power estimation using genetic spot optimization for large VLSI circuits
Michael S. Hsiao
January 1999 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(170.63 KB) Additional Information: full citation, index terms

11 Virtual simulation of distributed IP-based designs
Marcello Dalpasso, Alessandro Bogliolo, Luca Benini
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(732.16 KB) Additional Information: full citation, references, citings, index terms

12 Packetized On-Chip Interconnect Communication Analysis for MPSoC
Terry Tao Ye, Luca Benini, Giovanni De Micheli
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

Full text available: pdf(478.23 KB) Publisher Site
Additional Information: full citation, abstract, citings, index terms

Interconnect networks play a critical role in shared memory multi-processor systems-on-chip (MPSoC) designs. MPSoC performance and power consumption are greatly affected by the packet dataflows that are transported on the network. In this paper, by introducing a packetized on-chip communication power model, we discuss the packetization impact on MPSoC performance and power consumption. Particularly, we propose a quantitative analysis method to evaluate the relationship between different design o ...

13 Bidwidth analysis with application to silicon compilation
Mark Stephenson, Jonathan Babb, Saman Amarasinghe
May 2000 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2000 conference on Programming language design and implementation**, Volume 35 Issue 5

Additional Information: full citation, abstract, references, citings, index

Full text available: pdf(930.97 KB) terms

This paper introduces Bitwise, a compiler that minimizes the bitwidth the number of bits used to represent each operand for both integers and pointers in a program. By propagating 70 static information both forward and backward in the program dataflow graph, Bitwise frees the programmer from declaring bitwidth invariants in cases where the compiler can determine bitwidths automatically. Because loop instructions comprise the bulk of dynamically executed instructions, Bitw ...

14 Design methodologies meet network applications: Analysis of power consumption on switch fabrics in network routers

Terry Tao Ye, Giovanni De Micheli, Luca Benini

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(565.86 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we introduce a framework to estimate the power consumption on switch fabrics in network routers. We propose different modeling methodologies for node switches, internal buffers and interconnect wires inside switch fabric architectures. A simulation platform is also implemented to trace the dynamic power consumption with bit-level accuracy. Using this framework, four switch fabric architectures are analyzed under different traffic throughput and different numbers of ingress/egress ...

Keywords: interconnect networks, networks on chip, power consumption, systems on chip

15 Code compression for low power embedded system design

Haris Lekatsas, Jörg Henkel, Wayne Wolf

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(427.36 KB) Additional Information: full citation, abstract, references, citings, index terms

We propose instruction code compression as an efficient method for reducing power on an embedded system. Our approach is the first one to measure and optimize the power consumption of a complete SOC (System--On--a--Chip) comprising a CPU, instruction cache, data cache, main memory, data buses and address bus through code compression. We compare the pre-cache architecture (decompressor between main memory and cache) to a novel post-cache architecture (decompressor between cache and C ...

16 Routing and MAC: Versatile low power media access for wireless sensor networks

Joseph Polastre, Jason Hill, David Culler

November 2004 **Proceedings of the 2nd international conference on Embedded networked sensor systems**

Full text available: pdf(529.51 KB) Additional Information: full citation, abstract, references, citings, index terms

We propose B-MAC, a carrier sense media access protocol for wireless sensor networks that provides a flexible interface to obtain ultra low power operation, effective collision avoidance, and high channel utilization. To achieve low power operation, B-MAC employs an adaptive preamble sampling scheme to reduce duty cycle and minimize idle listening. B-MAC supports on-the-fly reconfiguration and provides bidirectional interfaces for system services t ...

Keywords: communication interfaces, energy efficient operation, media access protocols, networking, reconfigurable protocols, wireless sensor networks

17 Fast, flexible, cycle-accurate energy estimation
Phillip Stanley-Marbell, Michael Hsiao
August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**
Full text available: pdf(208.47 KB) Additional Information: full citation, references, citings, index terms

18 Activity-sensitive architectural power analysis for the control path
Paul E. Landman, Jan M. Rabaey
April 1995 **Proceedings of the 1995 international symposium on Low power design**
Full text available: pdf(83.91 KB) Additional Information: full citation, references, citings, index terms

19 RL-huffman encoding for test compression and power reduction in scan applications
Mehrdad Nourani, Mohammad H. Tehranipour
January 2005 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 10 Issue 1
Full text available: pdf(321.93 KB) Additional Information: full citation, abstract, references, index terms

This article mixes two encoding techniques to reduce test data volume, test pattern delivery time, and power dissipation in scan test applications. This is achieved by using run-length encoding followed by Huffman encoding. This combination is especially effective when the percentage of don't cares in a test set is high, which is a common case in today's large systems-on-chips (SoCs). Our analysis and experimental results confirm that achieving up to an 89&percent; compression ratio and a 93&per ...

Keywords: Compression ratio, Huffman encoding, decompression, power reduction, run-length encoding, scan applications, scan-in test power, switching activities, test compression, test pattern compression

20 Power: Predictive dynamic thermal management for multimedia applications
Jayanth Srinivasan, Sarita V. Adve
June 2003 **Proceedings of the 17th annual international conference on Supercomputing**
Full text available: pdf(386.28 KB) Additional Information: full citation, abstract, references, citings, index terms

Dynamic Thermal Management (DTM) techniques have been proposed to save on thermal packaging and cooling costs for general-purpose processors. However, when invoked, these techniques result in a significant performance degradation. This paper concerns performance-effective DTM for multimedia applications. We make two contributions: (1) Current DTM algorithms are **reactive** in nature. We propose a **predictive** DTM algorithm targeted at multimedia applications, which allows the efficient ...

Keywords: adaptive architectures, low power, thermal management

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IEE CNF	IEE Conference Proceeding
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2. **Pearl: a CMOS timing analyzer**
Cherry, J.J.;
Design Automation Conference, 1988. Proceedings., 25th ACM/IEEE
12-15 June 1988 Page(s):148 - 153
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